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Control of a Modular Multi-level Converter STATCOM for Low Voltage Ride-Through Condition

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Abstract—This paper presents a simulation study on the implementation of the Single Star Flying Capacitor Converter Modular Multi-level Cascaded Converter (MMCC-SSFCC) as a STATCOM operating under voltage sag condition. This paper proposes a cluster balancing control, using a zero sequence voltage injection technique for the SSFCC-STATCOM operating either as a reactive compensator under Low Voltage Ride Through condition (LVRT) or unbalanced current compensator. This control strategy enables the STATCOM system to compensate for both positive sequence reactive and negative sequence currents. Not only does it compensate for the load demands, but also keep the module DC-link and flying capacitor voltages at their rated values.

Keywords—voltage sag; flying capacitor converter; modular multilevel cascaded converter; Static synchronous compensator

I. INTRODUCTION

In power distribution systems, voltage unbalance can take several forms including unequal magnitudes, presence of harmonics and unequal phase shift between voltages. This occurs as a result of; uneven distribution of loads such as single phase traction drives and electric locomotives; open wye and delta transformer banks; asymmetric transmission impedances; and blown fuses in three phase capacitor banks [1]. These unbalanced voltages in power system result in sags, swells and interruptions [2]. This unbalance Voltage has an adverse effect on equipment, system stability and power quality of power distribution system [3]. This in turn increases losses, reduces efficiency and decrease life span of equipment.

The Static Synchronous Compensator (STATCOM) plays a paramount role in reactive power control and voltage regulation in power systems. This has also been applied to overcome the problems of unbalance[4]. Recent development in the medium and high voltage power converters such as the Modular Multilevel Cascaded Converter using stacked H-bridge cell configuration (MMCC-SSBC) [5] enables STATCOM application in transmission network. With its modular nature the topology offers a number of benefits such as scalability by using its modular nature to extend to any voltage level required without the use of step-up transformers [6]. In addition it gives good waveform quality at low switching frequency. The switching and clamping devices in MMCC are rated at module power and voltage levels, enabling the use of lower rated components operating under reduced voltage stress.

It has been shown that the MMCC is capable of compensating reactive power under balanced conditions [7]. However, with the occurrence of a phase voltage sag, the voltages of the power network become asymmetrical, causing the MMCC module capacitor voltages drifting away from their nominal values, if not properly monitored results to STATCOM failure [8]. It is of paramount importance that the STATCOM is able to withstand the adverse effect of voltage unbalance at the point of operation. Authors in [9] presented a control scheme for ensuring proper operation of STATCOM under condition of low voltage ride through (LVRT), but the STATCOM topology used was a two-level PWM controlled voltage source converter. Authors in [8] and [10] proposed a LVRT technique for an MMCC-SSBC based STATCOM which can prevent module capacitor voltage drifts by injection of a zero sequence voltage to each phase limb.

This paper presents a new STATCOM with a different topology to the MMCC-SSBC, known as the Single Star Flying Capacitor Converter-based MMCC (MMCC-SSFCC). Each of the three phase limbs of the MMCC-SSFCC comprises a chained modules of three-level Full-bridge Flying Capacitor Converter (3L-FCC) synthesizing three voltage levels (0, $\pm 0.5V_{DC}$ and $\pm V_{DC}$)[11]. Each 3L-FCC consist of an outer dc-bus capacitor C_{DC1}, two flying capacitors C_a, C_b and eight switch-diode pairs. The voltage on C_{DC1} defines the module voltage rating as V_{DC} and this is twice the voltage rating of two flying capacitors, likewise their capacitance. This configuration offers benefit of more switching states and voltage levels per module. This MMCC-SSFCC-based STATCOM has been investigated for balanced voltage application [11], but, to the author's knowledge, no work has been reported on its operation under voltage sag conditions. This paper shows that this STATCOM is capable

of operating under grid voltage sag conditions, providing LVRT and eliminating the effects of voltage sag on the load, whilst maintaining the module capacitor voltage balance.

II. DC VOLTAGE IMBALANCE IN MODULAR MULTILEVEL CASCASED FLYING CAPACITOR CONVERTER

Fig.1 shows the circuit configuration of a three phase STATCOM using the MMCC-SSFCC.

Under balanced operation this MMCC-SSFCC-based STATCOM is able to mitigate the reactive power, but when voltage sag occurs it faces challenging issue. This is because the average active power flowing through the converter is non-zero during voltage unbalance, but the module capacitors for the chained modules do not allow circulating current flowing within the converter phase limbs, resulting in module DC voltage imbalance.

The non-zero active power can be analyzed as follows;
Under unbalanced operation, the PCC voltages and compensation reference currents are written in phasor form as:

$$\begin{aligned} v_a &= V_p\angle\varphi_{vp} + V_n\angle\varphi_{vn} \\ v_b &= V_p\angle(\varphi_{vp} - \frac{2\pi}{3}) + V_n\angle(\varphi_{vn} + \frac{2\pi}{3}) \\ v_c &= V_p\angle(\varphi_{vp} + \frac{2\pi}{3}) + V_n\angle(\varphi_{vn} - \frac{2\pi}{3}) \end{aligned} \quad (1)$$

$$\begin{aligned} i_{ra}^{*} &= I_P\angle\varphi_{iP} + I_n\angle\varphi_{in} \\ i_{rb}^{*} &= I_P\angle(\varphi_{iP} - \frac{2\pi}{3}) + I_n\angle(\varphi_{in} + \frac{2\pi}{3}) \\ i_{rc}^{*} &= I_P\angle(\varphi_{iP} + \frac{2\pi}{3}) + I_n\angle(\varphi_{in} - \frac{2\pi}{3}) \end{aligned} \quad (2)$$

Thus the total per phase active powers are expressed as:

$$\begin{aligned} p_a &= \Re[(V_p\angle\varphi_{vp} + V_n\angle\varphi_{vn})(I_P\angle\varphi_{iP} + I_n\angle\varphi_{in})] \\ &= \begin{pmatrix} V_P I_P\cos(\varphi_{vP} - \varphi_{iP}) + V_n I_n\cos(\varphi_{vn} - \varphi_{in}) + \\ V_P I_n\cos(\varphi_{vP} - \varphi_{in}) + V_n I_P\cos(\varphi_{vn} - \varphi_{iP}) \end{pmatrix} \\ p_b &= \Re[\begin{pmatrix} (V_P\angle(\varphi_{vP} - \frac{2\pi}{3}) + V_n\angle(\varphi_{vn} + \frac{2\pi}{3})) \\ (I_P\angle(\varphi_{iP} - \frac{2\pi}{3}) + I_n\angle(\varphi_{in} + \frac{2\pi}{3})) \end{pmatrix}] \\ &= \begin{pmatrix} V_P I_P\cos(\varphi_{vP} - \varphi_{iP}) + V_n I_n\cos(\varphi_{vn} - \varphi_{in}) + V_P I_n \\ \cos(\varphi_{vP} - \varphi_{in} + \frac{2\pi}{3}) + V_n I_p\cos(\varphi_{vn} - \varphi_{ip} - \frac{2\pi}{3}) \end{pmatrix} \\ p_c &= \Re[\begin{pmatrix} (V_P\angle(\varphi_{vP} + \frac{2\pi}{3}) + V_n\angle(\varphi_{vn} - \frac{2\pi}{3})) \\ (I_P\angle(\varphi_{iP} + \frac{2\pi}{3}) + I_n\angle(\varphi_{in} - \frac{2\pi}{3})) \end{pmatrix}] \\ &= \begin{pmatrix} V_P I_P\cos(\varphi_{vP} - \varphi_{iP}) + V_n I_n\cos(\varphi_{vn} - \varphi_{in}) + V_P I_n \\ \cos(\varphi_{vP} - \varphi_{in} - \frac{2\pi}{3}) + V_n I_p\cos(\varphi_{vn} - \varphi_{ip} + \frac{2\pi}{3}) \end{pmatrix} \end{aligned} \quad (3)$$

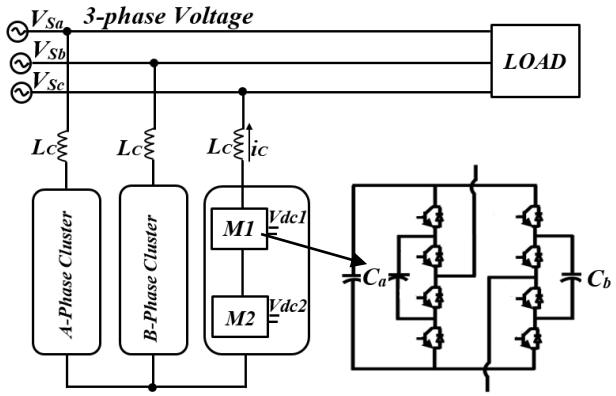

Fig. 1. Circuit configuration of the three phase MMCC-SSFCC STATCOM.

The first and second terms on the right-hand-side (RHS) of the above three expressions contain positive and negative sequence terms solely. These terms contribute the zero average active powers which are balanced. This implies that the average three phase power flowing through the STATCOM is zero. However the RHS third and last terms are cross products of positive sequence and negative sequence voltage and current respectively, they result in undesired non-zero average active power flowing through individual phases. This causes the DC link and flying capacitor voltages of each module drifting away from their nominal values. Hence, preventing the STATCOM to function properly as a reactive power compensator.

An effective approach to overcome this problem involves adding a common zero-sequence voltage to each of the three converter-limb voltages. If accurately estimated and applied to each phase limb, this zero-sequence voltage cancels out the effect of the cross component terms of each phase active power. Thus the control strategy for the MMCC-SSFCC-based STATCOM include the following:

1) DC link/cluster voltage balancing control
2) Zero-sequence voltage estimation
3) Converter reference voltage estimation

A. DC link/Cluster Voltage Balancing Control

The active power flowing through each phase limb ($\mathbf{P_a}$, $\mathbf{P_b}$ and $\mathbf{P_c}$) comprises two elements; the positive sequence active power owing to converter loss and negative sequence active power due to unbalanced voltage. Both must be compensated to prevent the phase limb voltages (module DC-link and flying capacitor voltages) deviating from their rated values. For the converter losses, the DC-bus voltage feedback control is applied as illustrated in Fig. 2. For MMCC-SSFCC topology obtaining the average value, $\mathbf{V_{DC\_avg}}$, of the three phase-limb DC-link voltages requires calculating per phase limb average DC voltage. This can be done by averaging the measured individual module voltages within the corresponding phase chain, so the DC-link average voltage for each phase is given as:

$$V_{DC\_(abc)} = \frac{1}{n_{mp}} \sum_{i=1}^{n_{mp}} V_{DC\_i(abc)} \quad (4)$$

where $\mathbf{n_{mp}}$ denotes the number of modules per phase and the average voltage of the three phase-limb $\mathbf{V_{DC\_avg}}$ can be evaluated as:

$$V_{DC\_avg} = \frac{V_{DC\_a} + V_{DC\_b} + V_{DC\_c}}{3} \quad (5)$$

Applying the average voltage value and the required nominal voltage $\mathbf{V_{DC\_ref}}$ to the DC-bus voltage feedback P+I controller (Fig. 2), the current I_{d_ref} is evaluated for active power compensation.

For compensating the effect of the second element - the negative sequence active power relies on implementing a cluster voltage balancing control scheme since it is this power flowing in and out of each converter phase limb that causes the imbalance of the phase limb DC-link voltages. As shown in Fig. 3, this cluster voltage balancing control consists of three PI regulators respectively for each phase limb. The average voltage $\mathbf{V_{DC\_avg}}$ evaluated in (5) and the individual phase average voltages (i.e. $\mathbf{V_{DC\_a}}$, $\mathbf{V_{DC\_b}}$ and $\mathbf{V_{DC\_c}}$) as derived in (4) are applied in generating the phase cluster powers. These cluster powers are further applied to determine the zero sequence voltage to be injected.

B. Zero Sequence Voltage Estimation

Having evaluated the active power, $\mathbf{P_a}$, $\mathbf{P_b}$ and $\mathbf{P_c}$ flowing through each phase limb, a zero sequence voltage $\mathbf{v_o}$ can be derived. This follows the principle that the sum of active power caused by the injected zero sequence voltage and that of existing active power expressed by (3) should balance the cluster powers. Thus, the equations for power across each phase are written as:

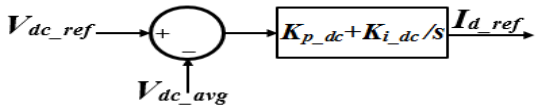

Fig. 2. DC link controller

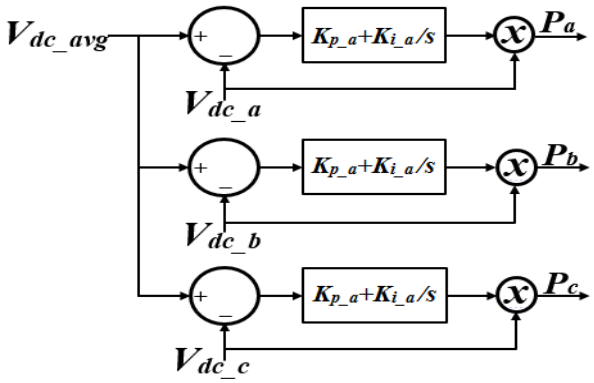

Fig. 3. Diagram of cluster voltage balancing control

$$\begin{aligned}
p_a &= \Re[(V_P\angle\varphi_{VP} + V_n\angle\varphi_{Vn} + V_0\angle\varphi_0)(I_P\angle\varphi_{iP} + I_n\angle\varphi_{in})] \\
&= \begin{pmatrix} V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in}) + \\ V_n I_P \cos(\varphi_{Vn} - \varphi_{iP}) + V_n I_n \cos(\varphi_{Vn} - \varphi_{in}) + \\ V_0 I_P \cos(\varphi_0 - \varphi_{iP}) + V_0 I_n \cos(\varphi_0 - \varphi_{in}) \end{pmatrix} \\
p_b &= \Re[\begin{pmatrix} (V_P\angle(\varphi_{VP} - \frac{2\pi}{3}) + V_n\angle(\varphi_{Vn} + \frac{2\pi}{3}) + V_0\angle\varphi_0) \\ (I_P\angle(\varphi_{iP} - \frac{2\pi}{3}) + I_n\angle(\varphi_{in} + \frac{2\pi}{3})) \end{pmatrix}] \\
&= \begin{pmatrix} V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in} + \frac{2\pi}{3}) + \\ V_n I_n \cos(\varphi_{Vn} - \varphi_{in}) + V_n I_P \cos(\varphi_{Vn} - \varphi_{ip} - \frac{2\pi}{3}) + \\ V_0 I_P \cos(\varphi_0 - \varphi_{iP} + \frac{2\pi}{3}) + + V_0 I_n \cos(\varphi_0 - \varphi_{in} - \frac{2\pi}{3}) \end{pmatrix} \\
p_c &= \Re[\begin{pmatrix} (V_P\angle(\varphi_{VP} + \frac{2\pi}{3}) + V_n\angle(\varphi_{Vn} - \frac{2\pi}{3}) + V_0\angle\varphi_0) \\ (I_P\angle(\varphi_{iP} + \frac{2\pi}{3}) + I_n\angle(\varphi_{in} - \frac{2\pi}{3})) \end{pmatrix}] \\
&= \begin{pmatrix} V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in} - \frac{2\pi}{3}) + \\ V_n I_n \cos(\varphi_{Vn} - \varphi_{in}) + V_n I_P \cos(\varphi_{Vn} - \varphi_{ip} + \frac{2\pi}{3}) + \\ V_0 I_P \cos(\varphi_0 - \varphi_{iP} - \frac{2\pi}{3}) + V_0 I_n \cos(\varphi_0 - \varphi_{in} + \frac{2\pi}{3}) \end{pmatrix}
\end{aligned} \quad (6)$$

To determine the amplitude and phase angle of $\mathbf{v_o}$, any two of three power equations in (6) can be used. Assuming the first two are selected they can be written as:

$$\begin{pmatrix} V_0 I_P \cos(\varphi_0 - \varphi_{iP}) + \\ V_0 I_n \cos(\varphi_0 - \varphi_{in}) \end{pmatrix} = p_a - \begin{pmatrix} V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in}) + \\ V_n I_n \cos(\varphi_{Vn} - \varphi_{in}) + V_n I_p \cos(\varphi_{Vn} - \varphi_{ip}) \end{pmatrix}$$

$$\begin{pmatrix} V_0 I_P \cos(\varphi_0 - \varphi_{iP} + \frac{2\pi}{3}) + \\ V_0 I_n \cos(\varphi_0 - \varphi_{in} - \frac{2\pi}{3}) \end{pmatrix} = p_b - \begin{pmatrix} [V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in} + \frac{2\pi}{3}) \\ + V_n I_n \cos(\varphi_{Vn} - \varphi_{in}) + V_n I_p \cos(\varphi_{Vn} - \varphi_{ip} - \frac{2\pi}{3})] \end{pmatrix}$$

(7)

and their more compact forms are given as:

$$\begin{aligned} X_{a1} V_0 \cos\varphi_0 + X_{a2} V_0 \sin\varphi_0 &= p_a - X_{a3} \\ X_{b1} V_0 \cos\varphi_0 + X_{b2} V_0 \sin\varphi_0 &= p_b - X_{b3} \end{aligned} \quad (8)$$

Where,

$$\begin{aligned}
X_{a1} &= I_p \cos\varphi_{ip} + I_n \cos\varphi_{in} \\
X_{a2} &= I_p \sin\varphi_{ip} + I_n \sin\varphi_{in} \\
X_{a3} &= \begin{pmatrix} V_P I_P \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in}) \\ + V_n I_n \cos(\varphi_{Vn} - \varphi_{in}) + V_n I_p \cos(\varphi_{Vn} - \varphi_{ip}) \end{pmatrix} \\
X_{b1} &= \left(I_p \cos(\varphi_{ip} - \frac{2\pi}{3}) + I_n \cos(\varphi_{in} + \frac{2\pi}{3}) \right)
\end{aligned}$$

$$X_{b2} = \left(I_p \sin(\varphi_{ip} - \frac{2\pi}{3}) + I_n \sin(\varphi_{in} + \frac{2\pi}{3}) \right)$$

$$X_{b3} = \begin{pmatrix} V_P I_p \cos(\varphi_{VP} - \varphi_{iP}) + V_P I_n \cos(\varphi_{VP} - \varphi_{in} + \frac{2\pi}{3}) \\ + V_n I_n \cos(\varphi_{Vn} - \varphi_{in}) + V_n I_p \cos(\varphi_{Vn} - \varphi_{ip} - \frac{2\pi}{3}) \end{pmatrix}$$

From (7) the zero sequence voltage amplitude and phase angle can be derived as:

$$V_0 = \frac{(p_a - X_{a3})}{X_{a1}\cos\varphi_0 + X_{a2}\sin\varphi_0} \quad (9)$$

$$\varphi_0 = \arctan\left[\frac{(p_a - X_{a3})X_{b1} - (p_b - X_{b3})X_{a1}}{(p_b - X_{b3})X_{a2} - (p_a - X_{a3})X_{b2}} \right] \quad (10)$$

and its time domain instantaneous voltage is expressed as

$$v_0 = V_0 \sin(\omega t + \varphi_0) \quad (11)$$

where $\theta = \omega t$ is the synchronous rotating angle created by the phase locked loop (PLL).

With the calculated zero sequence voltage applied to each phase, the average active power in all three phases should ideally be zero. This zero sequence voltage will not affect the values of voltage and current at the point of common coupling.

C. Converter Phase Reference Voltage Calculation

The reference voltage per phase limb of the converter should enable the current flowing to the PCC to compensate for reactive power under voltage sag condition. The current controller can be designed based on-

$$v_{c(abc)} = v_{s(abc)} - L_c \frac{di_{r(abc)}^*}{dt} - R i_{r(abc)}^* \quad (12)$$

Where $V_{s(abc)}$ are the 3-phase line to neutral voltages at PCC, $V_{c(abc)}$ are the 3-phase converter output voltages, $i_{r(abc)}$* are the 3-phase reference compensated currents. This method uses three voltage source current control for each phase of the converter. The voltage source current control is implemented using a predictive deadbeat control expressed as:

$$v_{c(abc)}(k+1) = v_{s\_(abc)}(k) - i_{r(abc)}^*(k)\left[\frac{L_c}{T_s}\right] - i_{c(abc)}(k)\left[R - \frac{L_c}{T_s}\right] \quad (13)$$

The three instantaneous converter line to neutral voltages including the zero sequence voltage ($V_{c\_(abc)}$ is expressed in (14) as:

$$v_{c\_(abc)} = v_{c(abc)} + v_o \quad (14)$$

Equation (14) ensures that with the addition of the calculated zero sequence voltage, the module capacitor voltages are maintained at their desired values. This scheme is verified with the DC-link and flying capacitors maintaining their desired values as discussed in section IV.

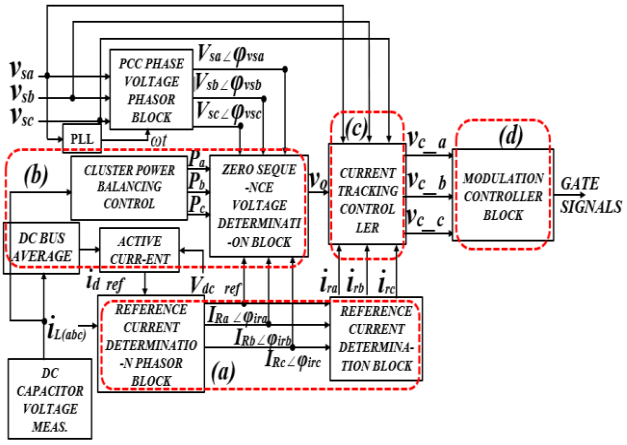

Fig. 4. Block diagram of MMCC-SSFCC STATCOM controller

III. MODULAR MULTILEVEL CASCASED FLYING CAPACITOR CONVERTER STATCOM CONTROL SCHEME

Fig. 4 shows the block diagram of the control system for the SSFCC-MMCC based STATCOM. This comprises four parts based on their respective functions, namely: (a) reference current determination block, (b) cluster voltage balancing control, (c) current tracking control and (d) modulator controller.

Under the reference current determination and cluster voltage balancing control block, the reference currents to be compensated are determined along with the cluster powers to estimate the zero sequence voltage to maintain the DC-link voltage at their nominal values. The current controller is used in generating the converter phase reference voltages. The current controller is actualized using the deadbeat predictive controller. The generated reference voltages are inputted into the modulator to synthesize gate signals. The phase shifted PWM is applied for this operation as discussed in [11].

IV. SIMULATION RESULTS

The proposed STATCOM controller is verified through simulation under voltage sag condition. The power system, STATCOM and control strategy are implemented via SIMULINK/MATLAB. All parameters are provided in table 1. Two different scenarios are studied to highlight the effectiveness of this STATCOM controller for MMCC-SSFCC.

A. STATCOM Low Voltage Ride Through Test Under Voltage Sag Condition

In this test, the controller performance when compensating for reactive power is analyzed under voltage sag condition. Fig. 5a shows the results for single phase voltage sag having a voltage depth of 100% for a duration of 100ms.

The voltage sag occurs when STATCOM is carrying out a reactive capacitive operation (reactive power Q=1.35KVAR). The STATCOM output voltage and current are shown in Fig.5b and 5c respectively.

TABLE 1
POWER SYSTEM CONFIGURATION PARAMETERS

parameters	Rating
Rated network line to neutral voltage (peak)	230V
Distribution system resistance	0.5Ω
Distribution system inductance	5mH
Filter resistance	20Ω
Filter inductance	1600μH
Rated Power System capacity	10KVA
Number of connected cells in per phase Nmp	2
Rated DC voltage of each module	150V
Rated DC voltage of module flying capacitor	75V
DC module capacitance rating	260μF
Module flying capacitor capacitance rating	130μF
Switching frequency fs	750Hz

The phase current has a 90^0 phase lead over the phase voltage. It can be observed that the compensated currents generated by STATCOM controller are balanced as seen in Fig. 5c, regardless of the voltage sag. With the injection of the proposed zero sequence voltage (Fig. 5f), it can be observed from Fig. 5d and 5e that the module and inner flying capacitor voltages has a deviation of around ±2V and ±4V respectively from their DC voltage reference. This is acceptable because it lies within its tolerance limit of ±10% voltage rating.

The effectiveness of the proposed balancing algorithm during asymmetric fault condition is compared with cluster balancing control without zero sequence voltage injection. Fig. 6 shows that the DC bus and inner flying capacitor voltages deviate from their desired values during fault ride through operation. This arises from the cross coupled power terms expressed in (3).

Fig. 7 shows the waveforms for three phase voltage sags with a voltage depth of 50%. The SSFCC based STATCOM continually inject three phase balanced sinusoidal currents for reactive power compensation even when voltage sag occurs (Fig. 7c). Fig. 7d and 7e show that the DC bus voltage and inner flying capacitor voltages are maintained at their nominal values. Under this symmetrical fault condition, all the dc bus and inner flying capacitor voltages are also maintained at their reference voltages even with the exclusion of the zero sequence voltage as seen in Fig. 8a and 8b respectively.

Regardless of both methods maintaining the module and inner flying capacitor voltages under symmetrical fault conditions, their behavior under asymmetrical fault condition differs. Therefore, the zero sequence voltage injection control method has better performance for fault ride through operations.

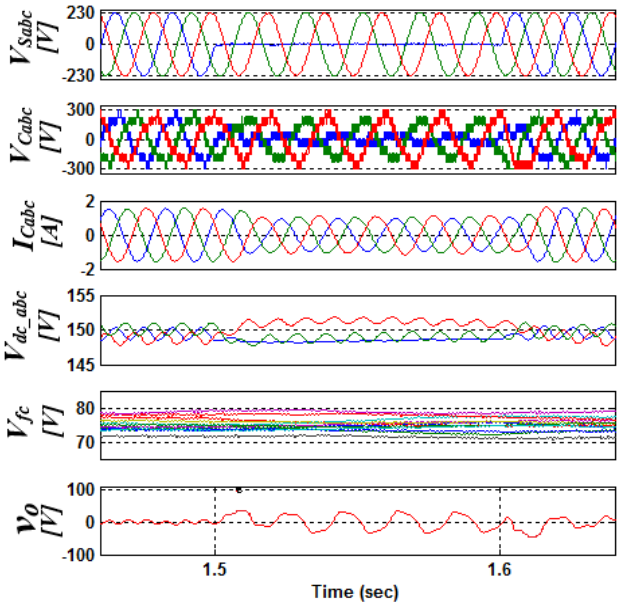

Fig. 5. Simulated waveforms during single phase voltage sag with a voltage depth of 100%. (a) Supply voltage. (b) Converter phase voltage. (c) STATCOM currents. (d) Module dc-link voltages. (e) Module flying capacitor voltage. (f) Zero sequence voltage

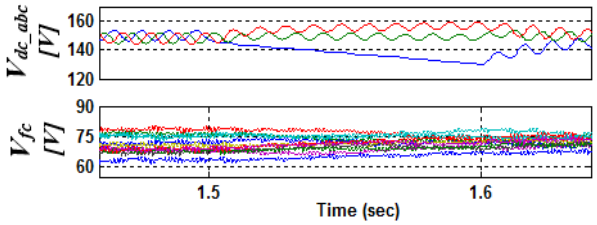

Fig. 6. Simulated waveforms during single phase voltage sag with a voltage depth of 100%. (a) Module dc-link voltages. (b) Module flying capacitor voltage.

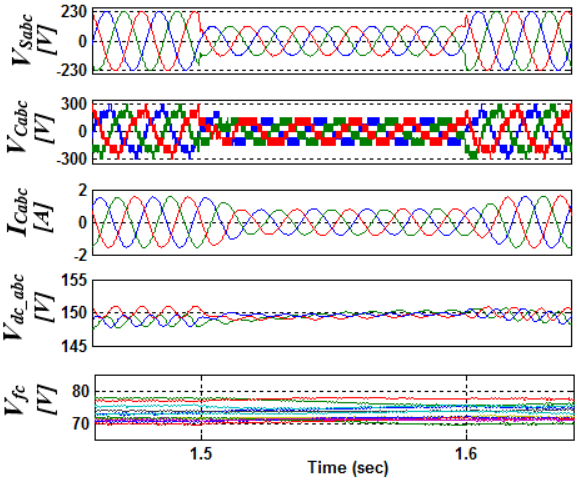

Fig. 7. Simulated waveforms during three phase voltage sag with a voltage depth of 50%. (a) Supply voltage. (b) Converter phase voltage. (c) STATCOM currents. (d) Module dc-link voltages. (e) Module flying capacitor voltage.

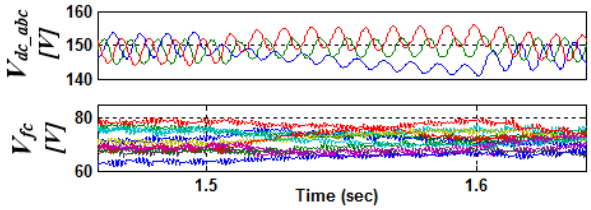

Fig. 8. Simulated waveforms during three phase voltage sag with a voltage depth of 50%. (a) Module dc-link voltages. (b) Module flying capacitor voltage.

B. STATCOM Reactive and Unbalanced Current Compensation Resulting From Unbalanced Voltage Condition

In this scenario, the STATCOM operation under unbalanced grid voltage is investigated. The system operates under balanced condition until at time t= 1.5s, an asymmetric fault (phase to ground fault) occurs at the supply side, resulting to a voltage depth of 50% (see Fig. 9a). After t= 1.5s, unbalanced current is absorbed by the balanced load as shown in Fig. 9c. This unbalanced condition created by the voltage sag is completely compensated by the STATCOM ensuring the current at the point of common coupling to be balanced and equal (see Fig. 9b). As a result of the voltage sag, a negative current component i_{Ln} = 0.4A and reactive current i_{Lq}= 1.4A is compensated by the STATCOM as seen in Fig. 9e and 9f respectively. This is completely compensated as the degree of unbalance created by the voltage sag at the load bus lies within the operating limit of the STATCOM controller:-

$$\frac{V_{DC\_(abc)} - V_{S(abc)}}{V_{S(abc)}} > \frac{i_{Ln}}{i_{Lq}} \qquad (15)$$

This implies that $0.3043 > 0.286$.

During the voltage sag, it is observed that module DC link voltages are maintained within their nominal values due to the cluster balancing control using the zero sequence voltage injection as seen in Fig. 9d.

CONCLUSION

This paper has discussed an MMCC-SSFCC based STATCOM operating under voltage sag condition using zero sequence voltage injection in achieving zero average power across each cluster. The simulation results have verified the LVRT capability of this converter based STATCOM enduring severe voltage sag conditions. Furthermore, this SSFCC-STATCOM has been operated to compensate for current imbalance introduced by the voltage sag condition. The module DC-link and flying capacitors of this converter do not show any divergence from their rated values or overshoot due to the voltage sag occurrence and restoration. This means that the proposed control system can handle asymmetric ac voltages and severe voltage sags.

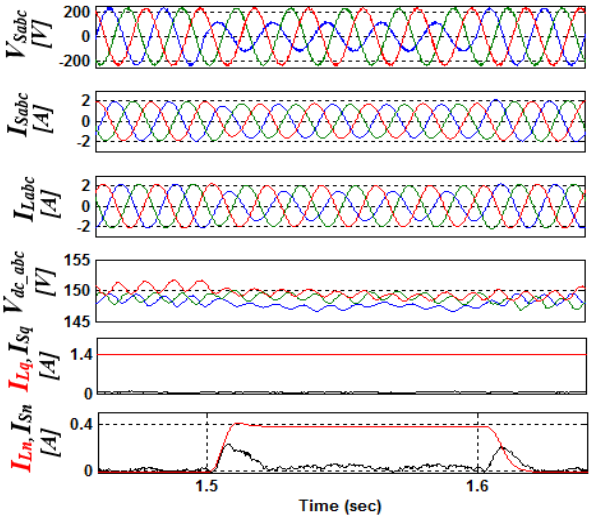

Fig. 9. Simulated waveforms during single phase voltage sag with a voltage depth of 50%. (a) Supply voltage. (b) Supply currents. (c) Load currents. (d) Module dc-link voltages. (e) Reactive current component: load reactive current $\mathbf{i_{Lq}}$ (red) and supply reactive current $\mathbf{i_{Sq}}$ (black). (f) Negative sequence current component: load negative sequence current $\mathbf{i_{Ln}}$ (red) and supply negative sequence current $\mathbf{i_{Sn}}$ (black).

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